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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,611	02/11/2002	Paul A. LaBerge	37829.0800/Micron 01-0357	6298

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EXAMINER	
BUTLER, DENNIS	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,611	LABERGE, PAUL A.	
	Examiner	Art Unit	
	Dennis M. Butler	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-34,36-39,41 and 42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-34, 36-39 and 41-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action is in response to amendment received on March 14, 2005. Claims 1, 3-34, 36-39 and 41-42 are pending.

2. The text of those sections of Title 35, US Code not included in this action can be found in a prior Office Action.

3. Claims 1, 3-34, 36-39 and 41-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Kuge, U. S. Patent 6,715,096.

Per claims 1, 8, 13, 19, 25, 31, 34 and 39:

A) Kuge teaches the following claimed items:

1. a memory controller controlling the transfer of data from a data source to a data destination with memory controller 2 of figure 1 and at column 8, lines 12-27 and 49-64;

2. a delay circuit generating a plurality of delayed clock signals at different times with delay line 22 of figure 9, with figures 10 and 13A, at column 14, lines 53-61, at column 15, lines 13-20 and at column 16, lines 17-30;

3. a plurality of latches responsive to the plurality of delayed clock signals, each latch receiving a timing signal from the data source and generating a latched signal with latch circuit 24 of figure 9, with figure 15, at column 14, line 62 – column 15, line 5, at column 15, lines 21-26 and at column 15, line 50 – column 16, line 16;

4. a comparing/analyzing circuit responsive to a plurality of latched signals from the plurality of latches that generates a comparison signal corresponding to a difference between the plurality of the latched signals, identifying a data valid

window (DVW), identifying a leading edge using a delay clock signal, a trailing edge using a delay clock signal and a midpoint of the DVW with the delay circuit 22, latch circuit 24, the strobe timing calculating circuit 26 and strobe timing storage circuit 5C of figure 9, with figures 15 and 17, at column 15, lines 1-13, at column 17, lines 4-35 and at column 18, line 60 – column 19, line 31.

Per claims 3-4, 9-10, 14-16, 21-22, 26, 33, 36, 38 and 41-42:

Kuge describes identifying a leading edge, a trailing edge and a midpoint of the DVW and adjusting the timing of at least one delay clock with the strobe timing calculating circuit 26 and strobe timing storage circuit 5C of figure 9, with figures 15 and 17, at column 15, lines 1-13, at column 17, lines 4-35 and at column 18, line 60 – column 19, line 31.

Per claims 5-7, 11-12, 17-18, 23-24, 27-28 and 30:

Kuge describes that the data source (memory) exhibits a voltage time constant (impedance) and the clock signal is delayed to compensate for the change in impedance at column 2, lines 10-22, at column 3, lines 3-20, at column 4, lines 16-27 and at column 4, line 56 – column 5, line 7. Kuge describes the delay circuit is a multi-tap delay line that generates the plurality of delay clock signals in conjunction with a free-running clock signal with clock generator 3 of figure 1, with delay line 22 of figure 9, with figures 10 and 13A, at column 14, lines 53-61, at column 15, lines 13-20 and at column 16, lines 17-30.

Per claims 20, 29, 32 and 37: